IN THE CLAIMS:

Please amend the claims as indicated in the complete listing of claims listed below. This listing of claims will replace all prior versions, and listings, of claims in the application:

1-52. (canceled)

53. (previously presented) A method of designing an integrated circuit (IC), said method comprising:

creating a representation of a shielding mesh in at least one layer of said IC, said shielding mesh having a first plurality of lines which are designed to provide a first reference voltage and having a second plurality of lines which are designed to provide a second reference voltage; and

creating a representation of a plurality of signal lines routed through said shielding mesh, wherein at least one of said signal lines is coupled to a signal line on another layer through at least two vias.

54. (previously presented) A method as in claim 53, wherein the method is performed at least in part by an EDA tool.

55. (previously presented) A method as in claim 54, wherein said method uses initial code written in an HDL.

56. (withdrawn) An integrated circuit (IC), comprising:

a shielding mesh having a first layer and a second layer, the first layer having a first conductor, the second layer having a second conductor; and

two vias each connecting from the first conductor of the first layer to the second conductor of the second layer.

57. (withdrawn) The integrated circuit of claim 56, wherein the first conductor and the second conductor are not parallel.

58. (withdrawn) The integrated circuit of claim 56, wherein the first conductor and the second conductor are in close proximity.

59. (withdrawn) The integrated circuit of claim 58, wherein a distance between the first conductor and the second conductor is smaller than an average spacing between parallel lines of the shielding mesh.

60. (currently amended) A method of designing an integrated circuit (IC), the method comprising:

generating a representation of at least one signal line;

generating a representation of a shielding mesh having a first layer and a second layer, the first layer including a first conductor, the second layer including a second conductor, wherein the shielding mesh shields said at least one signal line which is routed through the shielding mesh; and

generating a representation of two vias, each of the two vias connecting from the first conductor to the second conductor.

61. (previously presented) The method of claim 60, wherein the first conductor and the second conductor are not parallel.

62. (previously presented) The method of claim 60, wherein the first conductor and the second conductor are in close proximity.

63. (previously presented) The method of claim 62, wherein the method is performed at least in part by an EDA tool.

64. (withdrawn) A machine readable medium containing executable computer program instructions which when executed by a digital processing system cause said system to perform a method of designing an integrated circuit (IC), the method comprising:

generating a representation of a shielding mesh having a first layer and a second layer, the first layer including a first conductor, the second layer including a second conductor; and

generating a representation of two vias, each of the two vias connecting from the first conductor to the second conductor.

65. (withdrawn) The medium of claim 64, wherein the first conductor and the second conductor are not parallel.

66. (withdrawn) The medium of claim 64, wherein the first conductor and the second conductor are in close proximity.

67. (withdrawn) A data processing system for designing an integrated circuit (IC), the system comprising:

means for generating a representation of a shielding mesh having a first layer and a second layer, the first layer including a first conductor, the second layer including a second conductor; and

means for generating a representation of two vias, each of the two vias connecting from the first conductor to the second conductor.

68. (withdrawn) The system of claim 67, wherein the first conductor and the second conductor are not parallel.

69. (withdrawn) The system of claim 68, wherein the first conductor and the second conductor are in close proximity.

70. (new) The method of claim 53, wherein said shielding mesh is substantially confined in at least one of the following regions in said at least one layer: (a) a block, (b) a channel, or (c) an area made by at least four power lines.

71. (new) The method of claim 70, wherein said creating a representation of a shielding mesh is performed before routing a designed integrated circuit.

72. (new) The method of claim 60, wherein thickness of said first conductor is substantially the same as thickness of said at least one signal line.

73. (new) The method of claim 72, wherein an angle between a first direction along said first conductor and a second direction along said second conductor is substantially close to 90 degrees.

74. (new) The method of claim 60, wherein said first conductor is substantially close to a signal line from said at least one signal line, said signal line being substantially parallel to said first conductor.

75. (new) The method of claim 60, the method further comprising:

generating a representation of a power grid having a third layer and a fourth layer, said power grid comprising a plurality of power lines, wherein said third layer comprising a first power line and said fourth layer comprising a second power line and wherein said first conductor is coupled to said first power line and said second conductor is coupled to said second power line;

wherein a thickness of said first power line is substantially larger than a thickness of said first conductor.